STUDER D820 MCH
TLS-4000

INTERFACE DOCUMENTATION

Interface number : 1.812.435.21
IF - Doc number : 10.27.1930

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Summary

1 General Information

1.1 Ordering Information

	Order number
■ Interface Set (including interface, cable and documentation)	21.812.435.21
■ Interface board (Hardware/Software)	1.812.435.21
■ Hardware: TLS parallel interface	1.812.491.20
■ Software Set	1.812.974.21
■ IF-Cable 5m	1.023.780.00
■ Interface Docu-number	10.27.1930
■ Hardware (parallel IF) Docu-number	10.27.3040

1.2 Slave Model

- STUDER D820 MCH
- Device with compatible connection: STUDER D820 MCH

1.3 Software

First release (index 20)	1.812.974.20 (24/91)
■ update: (index 21) new parameter for control algorithm	1.812.974.21 (35/91)

2 Installing Procedures

2.1 TLS 4000 Requirements

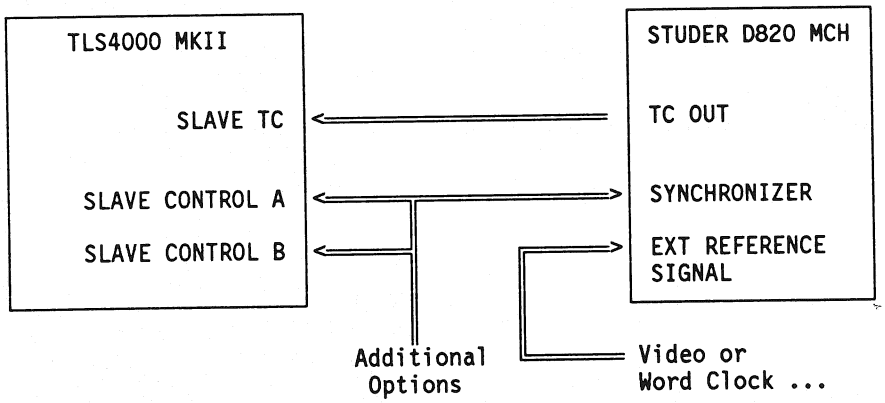
Order number

- Synchronizer Board — 1.812.320.25 or later
- Interface: — correct setup of the DIL switches (see 3.3)

2.2 Slave Requirements

- Slave software version 2.2
- Set the jumper on "TAPE DECK COUNTER/TIMER" board to position 64Hz.
  Set the "INT MOVE PULSE" in the setup menu to 64Hz.
  (refer to slave manual)
- Set the slave to the external synchronizer mode.
  (refer the slave manual)

2.3 Connection Slave-Synchronizer



2.4 Quick Test, Adjustments

Insert the Interface after switching off the synchronizer. Connect the slave machine and switch on synchronizer and slave.
During the first 5 seconds the interface will perform a short selftest. The result is commented with some led messages.
If no errors have been found, the display is available for operation messages (see section 3.5)

The correct wiring of movepulse information may easily be checked by disconnecting the slave timecode cable. The time display on the LCU or a controller should be updated with correct speed and direction.

A good timecode on tape is essential for synchronizer operation and should be checked for master and slave. Be shure that the time code was recorded with the same sampling rate as the audio signal.

No adjustments are necessary.

3 Operating Instructions

3.1 Technical Specifications

- Slave type:
  - Digital Audio Tape Recorder
  - SMPTE/EBU timecode with move information
  - GOTO with PLAY–STOP sequence
  - Chase–Stop with waiting in advance
  - transition Chase to Playsync with preparking
- Tapedeck Control:
  - by parallel communication
- Capstan control:
  - frequency 9.6kHz (nominal speed, samplingrate 48kHz)
- Movepulse information:
  - clock frequency 64Hz at nominal speed (48kHz)
  - direction: LOW = reverse
- Compensation of Record Dropin/out Delays:
  - compensated by synchronizer (includes both transmission delays and compensation of distance between erase and record head).
- Park accuracy:
  - typical 0.5 frames
- Lock time:

(in CUED status,	Master Start–UNMUTE):	< 6 sec
(in CHASE 10* vnom,	Master Start–UNMUTE):	< 12 sec

3.2 Summary of Supported Functions

Tape Deck Commands:

- STOP — a STOP command is sent
- PLAY, REC — nominal and external varispeed (±50%)
- EDIT — same as STOP
- FORW, REW — with toggle control from 0..max slave speed
- SHTLF, SHTLR — same as FORW/REW
- LOC, LOCREL — performed by interface
- REHEARSE: — implemented
- MUTE: — implemented
- EVENT Relay: — is available (see section 3.4)
- CONDITIONAL COMMANDS: — The timecode triggered execution is possible for the tape deck commands, the relay command and the audio mute and rehearse commands.
- STATUS Request: — Status information is updated periodically by means of parallel communication.
- AUDIO Channel Control: — not implemented.
- TRANSPARENT Commands: — not implemented.
- KEYBOARD DISABLE: — not implemented.

3.3 DIL-Switch Functions

DIL-Switch SZ81 allows the setting of some general modes.

- Switch 1: RECORD ENABLE
  Defines the polarity of RECEN (see section 3.4)
  OFF : RECORD enabled when
  - low level at RECEN pin

  ON : RECORD enabled when
  - high level at RECEN pin or input open

- Switch 2: REHEARSAL MODE
  If the rehearsal mode is active, RECORD commands will be
  OFF : replaced by PLAY commands
  ON : directly passed to the slave
  This switch should be in ON position.

- All other switches are not used and should be in OFF position.

- Default Settings: all switches in OFF position except switch 2

3.4 Additional Features at Slave Control B Connector

RECEN (PIN 2):
This signal is used to enable/disable the RECORD function with an external hardware. According to DIL-Switch position 1 and the level of the signal RECEN, RECORD commands are passed to the slave or modified to PLAY.

REL1 (PIN6), REL2 (PIN7):
A general purpose relay is controlled by EVON/EVOFF commands. The switch REL1/REL2 is closed with the command EVON.

BR-REHSL (PIN8), SR-REHSL (PIN13):
The rehearse mode can be activated by a low level at SREHSL. B-REHR as tally is active when the rehearse mode is switched on (by SREHSL or with a serial command from the synchronizer).

MVCL (PIN21), MVDR (PIN24):
This output provides buffered movepulse information to supply further synchronizer with master movepulses.

direction MVDIR: LOW = forward
frequency MVCL: 64Hz (48kHz samplingrate)

XVSENB/XVSREF (PIN 5, PIN 3):
An external varispeed circuit can be connected to the TLS. The two signals are switched to the slave during the OFF mode of the synchronizer.

enable varispeed XVSENB: LOW = enabled
reference frequency XVSREF: 9600Hz nominal (48kHz)

3.5 LED Diagnostic Display

Three LEDs are situated at the front of the interface board. They provide information about the result of the initial selftest and the online status.

DL 1 2 3 **(front view)**
(# = LED blinking, - = LED off, * = LED on)

- An initialization procedure is executed after reset and the main hardware devices are tested. Any resulting error is signalled with a blinking left LED (DL1, about 1 Hz).

- If all LEDs are blinking, the internal EEPROM of the processor has to be reconfigured. This should only happen if the processor was replaced and the interface switched on for the first time. If this happend, you have to switch JS 1 to position AB and reset the interface (power off - power on). After the initialisation the three LEDs should blink again. Put JS 1 back to position BC and reset the interface again.
  Now the 68HC11 shold be reconfigured and the LED message should not be the same.

DL1	DL2	DL3	
#	-	-	CPU RAM test failed.
#	-	*	RAM test failed.
#	*	-	SSDA test failed.
#	#	#	Microprocessor 68HC11 has to be reconfigured

- If no error was found, DL1 stays dark and the other two LEDs light, if communication with the slave or the synchronizer fails.

DL1	DL2	DL3	
-	*	*	no connection with the synchronizer board
-	*	-	no connection with the SLAVE
-	-	*	slave error (ex: tape out)

- If the left LED is on, a fatal processor error has occurred. A reset is necessary to return to operation mode. The interface board should be checked whenever such an error was encountered.
  In this case the interface should be resetted and this error message should not occur anymore.

DL1	DL2	DL3	
*	–	–	Fatal soft- or hardware error (eg ROM defect)
*	–	*	Watch dog error
*	*	–	Clock error
*	*	*	Illegal opcode

3.6 Application Hints

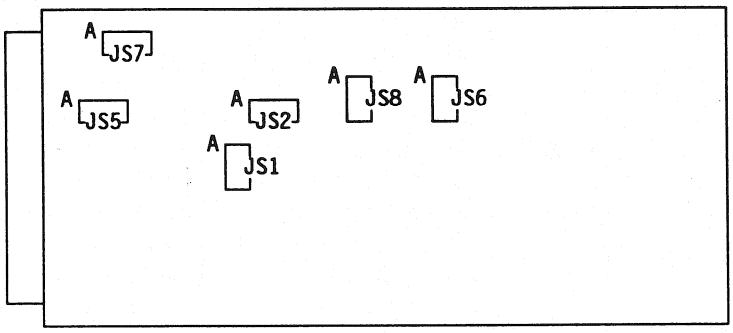
- The interface is able to recognize the sample frequency of the used tape. If you use a new tape with a different sampling rate, set the D820 MCH to "play" for about 5 seconds. During this time the correct acknowledgment will be done.

- It is recommended not to use the parallel remote control connector for the varispeed function with the synchronizer. Use the XVS input on the synchronizer control B connector. Otherwise conflict between the synchronizer and the varispeed device could occur.
  (Refer to section 3.4 for more information)

- Remote switching of the synchronizer from the slave machine is available.

4 Service Instructions

4.1 Jumper Settings



Function of the jumpers:

	Position AB	Position BC
JS1	Processor in special test mode	Processor in normal expanded mode *
JS2	PE6 input of the processor is LOW	PE6 input of the processor is HIGH *
JS5	IF ground is connected to the slave ground *	No connection between IF ground and slave ground
JS6	Capstan reference output has no pullup resistor	Capstan reference output has a pullup resistor *
JS7	Opto isolated inputs are supplied from the IF *	Opto isolated inputs are supplied from the slave
JS8	Capstan pullup resistor is supplied with 5V (or MVCC if JS7 'AB')	Capstan pullup resistor is supplied with 15V *

* default settings for D820 MCH

4.2 Signal Description, Slave Connectors

SLAVE CONTROL A:

Pin	Signal	Type	Slave Sig.	Description
1	MGND		+0.0	ground of D820 MCH
2	PAIN1		BR-RWD	Rewind status
3	PAIN2		BR-FORW	Forward wind status
4	PAIN6		BR-VRSPD	varispeed status
5	CAPEN	I out	SR VRSPD	capstan varispeed enable (LOW = enb)
6	-		-	(not used)
7	MOVCL	I in	OR-MVCLK	move signal clock from D820 MCH
8	-		-	(not used)
9	PAIN5		BR-REC	Record status
10	MOVDIR	I in	OR-MVDIR	move signal direction from D820 MCH LOW = rewind
11	+5V		-	(not used)
12	0.0V		0.0V	screen
13	CAPCL	I out	IR-FEFEX	capstan clock (9600Hz nominal)
14	-		-	(not used)
15	PAIN3		BR-PLAY	Play status
16	PAIN4		BR-STOP	Stop status
17	PAOUT7		SR-MUTE	Mute command
18	PAOUT8		SR-LIFT	Lifter command
19	PAOUT5		SR-REC	Record command
20	PAOUT1		SR-REW	Rewind command
21	PAOUT2		SR-FORW	Forward wind command
22	PAOUT3		SR-PLAY	Play command
23	PAOUT4		SR-STOP	Stop command
24	-		-	(not used)
25	MVCC	+ 24 V	+ 24.0	supply voltage of D820 MCH

I out logic output, active low
(open collector, max 30V/0.3A)
I in logic input, active low, optoisolated
(I-low > 10 mA)

SLAVE CONTROL B:

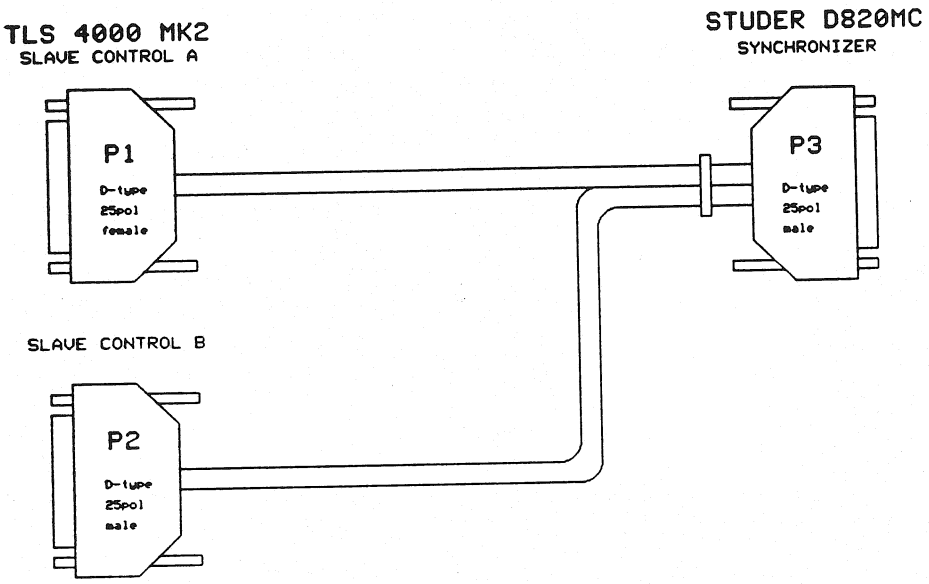
Pin	Signal	Type	Slave Sig.	Description
1	0.0V			signal ground
2	RECEN/PAIN11	I in		record enable / safe input (see DIL Switch 81.1)
3	XVSREF/PAIN10			external varispeed frequency
4	-			(not used)
5	XVSENB/PAIN9	I in		external varispeed enable
6	REL1			event relay contact 100V/0.3A
7	REL2			event relay contact 100V/0.3A
8	PAOUT6	I out	SR-REHSL	rehearsal on indication
9	PAOUT7			
10	PAOUT8			
11	+5V			TLS supply voltage
12	PAIN12	I in	OR-SYENB	sync. enable status
13	PAIN13	I in		rehearsal input
14	DC			(not used)
15	-			(not used)
16	PAIN14			(not used)
17	PAIN15			(not used)
18	PAIN16			(not used)
19	PAIN7			(not used)
20	0.0V			(not used)
21	MVCL	I out		move signal clock (9600Hz nominal)
22	-			(not used)
23	-			(not used)
24	MVDR	I out		move signal direction (LOW = FORW)
25	0.0V			(not used)

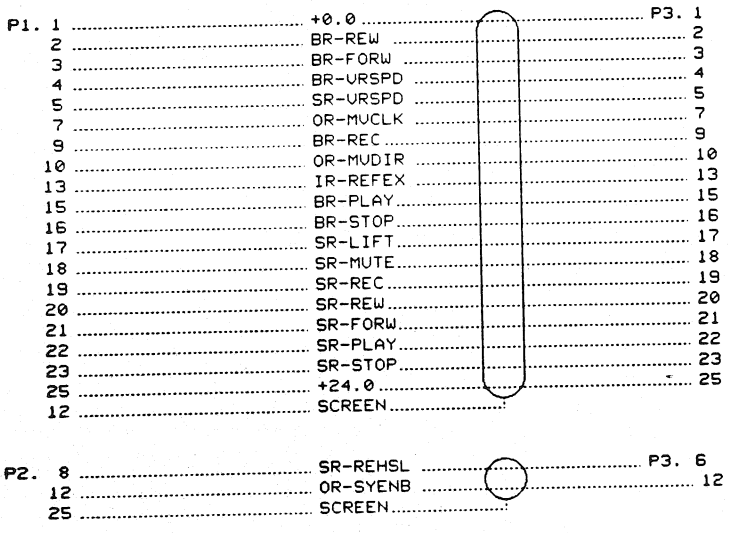
I out logic output, active low
(open collector, max 30V/0.3A)

I in logic input, active low, optoisolated
(I-low > 10 mA)

Remark: Schematics → see universal parallel IF

4.3 IF Cable Description





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STUDER INTERNATIONAL	TLS-4000 M2			PAGE 1 OF 1
	IF-KABEL STUDER D820MCH	5M	4H	1.023.780.00